This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of distributing packets among a plurality of ~~processing devices~~ cache systems, the method comprising:

configuring a content addressable memory (CAM) to indicate distribution of received packets based on a load balancing technique to a plurality of cache systems that each spoof a destination indicated by the received packets;

receiving a packet;

inputting at least a portion of the packet into CAM ~~a content addressable memory~~; and

obtaining a result from the ~~content addressable memory (CAM)~~ CAM to indicate whether to redirect the received packet to a selected ~~processing device~~ cache system and to indicate to which ~~processing device~~ cache system selected from among the plurality of ~~processing devices~~ cache systems the received packet is to be redirected if the CAM also indicates that the received packet is to be redirected~~, wherein the CAM is configured to distribute received packets to the plurality of processing devices based on a load balancing technique~~;

redirecting the received packet to the selected ~~processing device~~ cache system when the CAM indicates to redirect the received packet; and

sending the received packet to a destination indicated by the received packet when the CAM does not indicate to redirect the received packet.

2. (cancelled)

3. (original) A method as recited in claim 1, wherein the result indicates to redirect the packet from being sent to a destination specified in the received packet.

4. (currently amended) A method as recited in claim 3, wherein the result includes a ~~processing device~~ cache system device identification corresponding to the selected device to which the received packet is to be sent.

5. (original) A method as recited in claim 1, wherein the content addressable memory is a ternary content addressable memory.

6. (original) A method as recited in claim 1, wherein the portion(s) of the received packet input into the content addressable memory is selected from a group consisting of a destination address, a destination port, a source address, a source port, and a protocol.

7. (original) A method as recited in claim 1, wherein the TCAM includes a plurality of entries, and each entry includes a bits-to-match field, an action field, and a redirection destination field.

8. (original) A method as recited in claim 7, wherein the redirection destination field identifies a cache system.

9. (original) A method as recited in claim 8, wherein the action field indicates whether the received packet is to be redirected.

10. (currently amended) A method for facilitating traffic distribution among a plurality of devices, the method comprising generating a plurality of entries within a content addressable memory, each entry including a set of bit values that correspond to at least a portion of a packet and each entry including one or more destination fields indicating where to send a packet that matches the entry's set of bit values and indicating whether to redirect the packet

from a destination indicated by the packet, wherein the CAM is configured to distribute received packets to the plurality of ~~processing devices~~ cache systems based on a load balancing technique.

11. (original) A method as recited in claim 10, wherein the destination fields include an action field indicating whether to redirect the packet from a destination indicated by the packet itself.

12. (original) A method as recited in claim 11, wherein the destination fields include a destination identifier indicating a device to which the packet is to be redirected.

13. (original) A method as recited in claim 10, wherein the set of bits values include at least a 1 or a 0 value and a "don't care" value.

14. (original) A method as recited in claim 10, wherein the content addressable memory is ternary.

15. (currently amended) A computer system operable to distribute packets among a plurality of ~~processing devices~~ cache systems, comprising:

a first memory;

a content addressable memory; and

a processor coupled to the first memory and the content addressable memory, wherein at least one of the first memory and the processor are adapted to provide:

configuring a content addressable memory (CAM) to indicate distribution of received packets based on a load balancing technique to a plurality of cache systems that each spoof a destination indicated by the received packets;

receiving a packet;

inputting at least a portion of the packet into the content addressable memory; and

obtaining a result from the content addressable memory (CAM) to indicate whether to redirect the received packet to a selected ~~processing device~~ cache system and to indicate to which ~~processing device~~ cache system selected from among the plurality of ~~processing devices~~ cache systems the received packet is to be redirected if the CAM also indicates that the received packet is to be redirected, wherein the CAM is configured to distribute received packets to the plurality of ~~processing device~~ cache systems based on a load balancing technique;

redirecting the received packet to the selected ~~processing device~~ cache system when the CAM indicates to redirect the received packet; and

sending the received packet to a destination indicated by the received packet when the CAM does not indicate to redirect the received packet.

16. (original) A computer system as recited in claim 15, wherein the selected device is selected from a plurality of cache systems.

17. (original) A computer system as recited in claim 15, wherein the result indicates to redirect the packet from being sent to a destination specified in the received packet.

18. (currently amended) A computer system as recited in claim 17, wherein the result includes a ~~processing device~~ cache system identification corresponding to the selected ~~device~~ cache system to which the received packet is to be sent.

19. (original) A computer system as recited in claim 15, wherein the content addressable memory is a ternary content addressable memory.

20. (original) A computer system as recited in claim 15, wherein the at least a portion of the received packet is selected from a group consisting of a destination address, a destination port, a source address, a source port, and a protocol.

21. (original) A computer system as recited in claim 15, wherein the content addressable memory includes a plurality of entries, and each entry includes a bits-to-match field, an action field, and a redirection destination field.

22. (original) A computer system as recited in claim 21, wherein the redirection destination field identifies a cache system.

23. (original) A computer system as recited in claim 22, wherein the action field indicates whether the received packet is to be redirected.

24. (currently amended) A computer system operable to facilitate traffic distribution among a plurality of ~~devices~~ cache systems, comprising:

a first memory;

a content addressable memory; and

a processor coupled to the first memory and the content addressable memory (CAM),

wherein at least one of the first memory and the processor are adapted to provide generating a plurality of entries within the content addressable memory, each entry including a set of bit values that correspond to at least a portion of a packet and each entry including one or more destination fields indicating where to send a packet that matches the entry's set of bit values and indicating whether to redirect the packet from a destination indicated by the packet, wherein the CAM is configured to distribute received packets to the plurality of ~~devices~~ cache systems based on a load balancing technique.

25. (original) A computer system as recited in claim 24, wherein the destination fields include an action field indicating whether to redirect the packet from a destination indicated by the packet itself.

26. (currently amended) A computer system as recited in claim 25, wherein the destination fields include a destination identifier indicating a ~~device~~ cache sytem to which the packet is to be redirected.

27. (original) A computer system as recited in claim 24, wherein the set of bits values include at least a 1 or a 0 value and a "don't care" value.

28. (original) A computer system as recited in claim 24, wherein the content addressable memory is ternary.

29. (currently amended) A computer program product for distributing traffic, the computer program product comprising:

at least one computer readable medium;

computer program instructions stored within the at least one computer readable product configured to cause a ~~processing device~~ cache system to:

configure a content addressable memory (CAM) to indicate distribution of received packets based on a load balancing technique to a plurality of cache systems that each spoof a destination indicated by the received packets;

receive a packet;

input at least a portion of the packet into a content addressable memory; and

obtain a result from the content addressable memory (CAM) to indicate whether to redirect the received packet to a selected ~~processing~~

~~device~~ cache system and to indicate to which ~~processing device~~ cache system selected from among the plurality of ~~processing devices~~ cache systems the received packet is to be redirected if the CAM also indicates that the received packet is to be redirected, wherein the CAM is configured to distribute received packets to the plurality of ~~processing devices~~ cache systems based on a load balancing technique;

redirect the received packet to the selected ~~processing device~~ cache system when the CAM indicates to redirect the received packet; and

send the received packet to a destination indicated by the received packet when the CAM does not indicate to redirect the received packet.

30. (currently amended) A computer program product for distributing traffic, the computer program product comprising:

at least one computer readable medium;

computer program instructions stored within the at least one computer readable product configured ~~to cause a processing device~~ to generate a plurality of entries within a content addressable memory, each entry including a set of bit values that correspond to at least a portion of a packet and each entry including one or more destination fields indicating where to send a packet that matches the entry's set of bit values and indicating whether to redirect the packet from a destination indicated by the packet, wherein the CAM is configured to distribute received packets to a plurality of devices based on a load balancing technique.

31. (currently amended) An apparatus for distributing traffic comprising:

a means for configuring a content addressable memory (CAM) to indicate distribution of received packets based on a load balancing technique to a plurality of cache systems that each spoof a destination indicated by the received packets;

a means for receiving a packet;

a means for inputting at least a portion of the packet into a content addressable memory; and

a means for obtaining a result from the content addressable memory to indicate whether to redirect the received packet to a selected ~~processing device~~ cache system or to forward the received packet to a destination specified by the received packet and to indicate to which ~~processing device~~ cache system selected from among the plurality of ~~processing devices~~ cache systems the received packet is to be redirected if the CAM also indicates that the received packet is to be redirected, wherein the CAM is configured to distribute received packets to the plurality of ~~processing devices~~ cache sytems based on a load balancing technique; and

a means for sending the received packet to the indicated ~~processing device~~ cache system.

32. (currently amended) An apparatus for distributing traffic comprising a means for generating a plurality of entries within a content addressable memory, each entry including a set of bit values that correspond to at least a portion of a packet and each entry including one or more destination fields indicating where to send a packet that matches the entry's set of bit values and indicating whether to redirect the packet from a destination indicated by the packet, wherein the CAM is configured to distribute received packets to the plurality of ~~processing devices~~ cache systems based on a load balancing technique.

33. (cancelled)

34. (previously presented) A computer program as recited in claim 29, wherein the result indicates to redirect the packet from being sent to a destination specified in the received packet.

35. (currently amended) A computer program as recited in claim 34, wherein the result includes a ~~processing device~~ cache system identification corresponding to the selected ~~device~~ cache system to which the received packet is to be sent.

36. (previously presented) A computer program as recited in claim 29, wherein the content addressable memory is a ternary content addressable memory.

37. (previously presented) A computer program as recited in claim 29, wherein the portion(s) of the received packet input into the content addressable memory is selected from a group consisting of a destination address, a destination port, a source address, a source port, and a protocol.

38. (previously presented) A computer program as recited in claim 29, wherein the TCAM includes a plurality of entries, and each entry includes a bits-to-match field, an action field, and a redirection destination field.

39. (previously presented) A computer program as recited in claim 38, wherein the redirection destination field identifies a cache system.

40. (previously presented) A computer program as recited in claim 39, wherein the action field indicates whether the received packet is to be redirected.